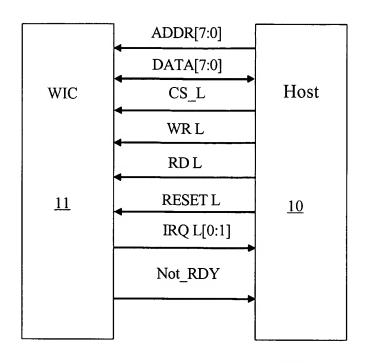
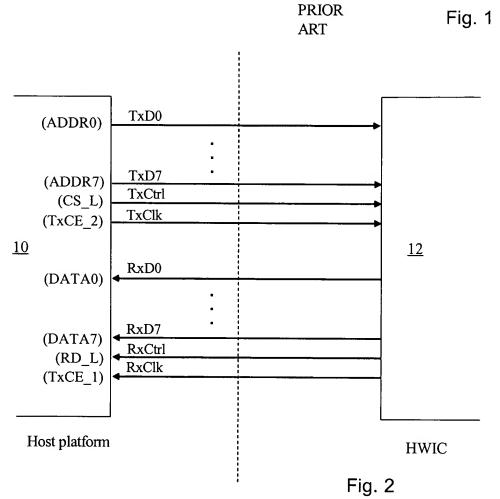
Title: BACKWARD-COMPATIBLE PARALLEL DDR BUS FOR USE IN HOST-DAUGHTERCARD INTERFACE

Inventor: James Everett Grishaw, et al. Attorney Docket No. 002-26: CSN 7523

SHEET <u>1</u> OF 5





Title: BACKWARD-COMPATIBLE PARALLEL DDR BUS FOR USE IN HOST-DAUGHTERCARD INTERFACE Inventor: James Everett Grishaw, et al. Attorney Docket No. 002-26: CSN 7523

SHEET 2 OF 5 14 15 Host Memory **CPU** (e.g. SDRAM, DDR, etc.) Fast Bus <u>10</u> Host Termination Logic <u>16</u> HWIC I/F Host 24 18 68 Pin WIC/VIC/HWIC I/F HWIC I/F - 22 **HWIC** <u>12</u> <u>20</u> **HWIC Termination Logic** Fig. 3

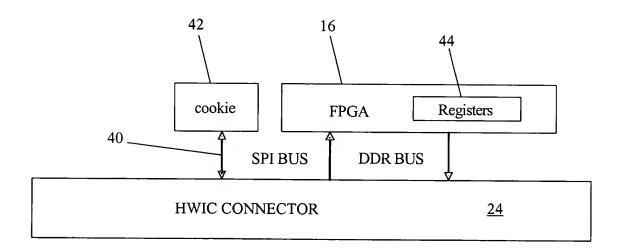


Fig. 4

Title: BACKWARD-COMPATIBLE PARALLEL DDR BUS FOR USE IN HOST-DAUGHTERCARD INTERFACE Inventor: James Everett Grishaw, et al.

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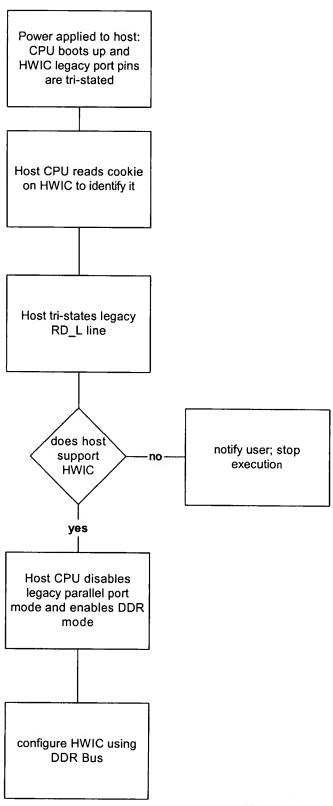


Fig. 5

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## SHEET $\frac{4}{\phantom{0}}$ OF 5

Command Opcode	Address	CRC8
0x01	32 Bits	8 bits

Fig. 6A

Command Opcode	Address	Data	CRC8
0x02	32 Bits	8 bits	8 bits

Fig. 6B

Command Opcode	Address	Data	CRC8
0x08	32 Bits	8 bits	8 bits

Fig. 7A

Command Opcode			
0x1F			

Fig. 7B

Command Opcode	Source	CRC8
0x0C	16 bits	8 bits

Fig. 8

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Command Opcode	Data	(Optional) Rx Flags	CRC8
0x11	N bytes	8 bits	8 bits

Fig. 9

DMA Read Opcode	Address	Length	CRC8
0x61	32 bits	16 bits	8 bits

Fig. 10

DMA Read Response Opcode	Address	Length	Header CRC8	Data	Frame CRC8
0x62	32 bits	16 bits	8 bits	"Length" bytes	8 bits

Fig. 11

DMA Write Opcode	Address	Length	Header CRC8	Data	Frame CRC8
0x66 or 0x67	32 bits	16 bits	8 bits	"Length" bytes	8 bits

Fig. 12